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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 042390.P7940 Total Pages 3

First Named Inventor or Application Identifier Boon-Lock Yeo

Express Mail Label No. EL 431 890 855 US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 20)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 5)

4. X Oath or Declaration (Total Pages 5)

a. x Newly Executed (**Original** or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ____ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. ____ Nucleotide and/or Amino Acid Sequence Submission

(if applicable, all necessary)

a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)

_X_ b. Power of Attorney

10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449

_____ b. Copies of IDS Citations

12. _____ Preliminary Amendment
13. _X_ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)

b. Statement filed in prior application, Status still proper and desired

15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. _____ Other: Certificate of Express Mail with copy of postcard showing contents of Express Mail package.

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

___ Continuation ____ Divisional ____ Continuation-in-part (CIP)

of prior application No: _____

18. **Correspondence Address**

_____ Customer Number or Bar Code Label _____
(Insert Customer No. or Attach Bar Code Label here)

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UNITED STATES PATENT APPLICATION

FOR

Method And Apparatus For Video Decoding On A Multiprocessor System

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METHOD AND APPARATUS FOR VIDEO DECODING ON A MULTIPROCESSOR SYSTEM

FIELD OF THE INVENTION

The present invention relates computers and multimedia processing, and, in particular, to the decoding compressed video on a multiprocessor system.

BACKGROUND OF THE INVENTION

Recent advances in computer technology have placed video applications within the reach of more common applications. For example, high Definition Television, Boradcast satellite Service, Cable TV distribution on optical networks, Electron Cinema, Interactive Storage Media, Multimedia Mailing, Networked Data base Services, corporate Internet training and conferencing, Remote Video Surveillance and others are now becoming practical video applications.

The large amounts of data needed to make video available in all these cases has lead to the adoption of Moving Picture Experts Group 1 (MPEG) and MPEG-2 standards for motion video compression and decompression. These standards significantly reduce bandwidth and storage space requirements. As a result, MPEG-1 and MPEG-2 are used in many video applications and are continuing to become more popular.

However, one feature limiting widespread use of the MPEG standard is it computational complexity. Video encoding and decoding under MPEG is expensive, often too costly for single processors to achieve real-time performance in software for displays of acceptable resolution and size. The computational demands grow as users desire higher quality video.

Encoding is more expensive than decoding, but can typically be done offline and, therefore, may not need to be done in real-time. Decoding, however, typically requires real-time performance.

SUMMARY OF THE INVENTION

The present invention provides a method and apparatus for decoding compressed video. The method includes reading a stream of compressed video into a memory. The video includes multiple pictures, with each picture having one or more independent elements. Thereafter, assigning, via a first processor of a group of processors sharing the memory, at least one independent element per processor to be decoded by the processors in parallel; and decoding the independent elements of the video stream in parallel.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates the hierarchy of layers in an MPEG bitstream.

Figure 2 illustrates a block diagram of encoding and decoding video data, according to one embodiment.

Figure 3 illustrates a block diagram of a picture slice structure.

Figure 4 illustrates a flow diagram describing the steps of decoding video data with multiple processors in parallel, according to one embodiment.

Figure 5 illustrates a multiprocessor computer system having a computer readable medium with instructions stored thereon according to one embodiment.

DETAILED DESCRIPTION

A method and apparatus for decoding compressed video on a multiprocessor system is disclosed. In the following description, for purposes of explanation, specific nomenclature is set forth to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention. For example, although the embodiments discussed below describe the present invention being used to decode video data encoded in accordance with the MPEG standard, alternative video encoding/decoding standards could be used without departing from the present invention.

MPEG Decoding

In its general form, an MPEG system stream is made up of two layers: the system layer contains timing and other information needed to demultiplex the audio and video streams and to synchronize audio and video during playback; and, the compression layer which includes the audio and video data streams.

One embodiment of the hierarchy of layers in an MPEG bitstream is arranged in the following order, as illustrated in Figure 1: Sequence, Group of Pictures (GOP), Picture Slice, Macroblock, and Block. The different parts of the stream are marked with unique, byte-aligned codes

called startcodes. These startcodes are used both to identify certain parts of the stream and to allow random access into the video stream.

The highest level in the layering is the sequence level. A sequence is made up of groups of pictures (GOPs). Each GOP is a grouping of a number of adjacent pictures. One purpose in creating such an identifiable grouping is to provide a point of random access into the video stream for play control functions (fast forward, reverse, etc.).

Within each GOP are a number of pictures. In MPEG-2 interlaced video is supported so each picture corresponds to either a frame (for progressive or interlaced video streams) or a field (for interlaced video streams) in the original stream.

Pictures are further subdivided into slices, each of which defines a fragment of a row in the picture. Slices comprise a series of macroblocks, which in one embodiment are 16x16 pixel groups containing the luminance and chrominance data for those pixels in the decoded picture.

Macroblocks are divided into blocks. A block in one embodiment is an 8x8-pixel group that further describes the luminance or chrominance for that group of pixels. Blocks are the basic unit of data at which the decoder processes the encoded video stream. Macroblocks and blocks do

not have startcodes associated with them; their boundaries are discovered implicitly while decoding.

Encoding

As described above, the block is the basic unit of data processing. As illustrated in Figure 2, in one embodiment for each block of data in the video sequence, the encoder typically performs following five steps to produce an encoded block: motion estimation, discrete cosine transform (DCT), quantization, and run-length and Huffman coding.

In the first stage, motion estimation, the encoder tries to take advantage of temporal redundancies among pictures. The next four stages of the encoder take advantage of spatial correlation in compressing the video sequence. The result of performing these five encoding stages on all blocks in a video-sequence is an MPEG encoded video stream. A stream may be encoded once and then transmitted across a transmission media and/or stored as needed. However, decoding is typically necessary each time the stream is viewed.

Decoding

The decoding process for an MPEG encoded stream typically performs the five encoding stages in reverse order. First Huffman and run-length decoding are applied to generate the quantized block. Then inverse quantization is performed to obtain the block's frequency

spectrum. From this, the inverse discrete cosine transform is taken. Then, if necessary, motion compensation may be used to generate the final macroblock of data from the prediction error, motion vectors, and reference picture.

A significant difference between the encoding and decoding processes is that in the former, much time is spent in motion estimation as it is necessary to search for the most similar macroblock in the reference picture(s), whereas in the latter, motion vectors are already available, which makes motion compensation much cheaper than motion estimation.

Decoding Video Data with Multiple Processors in Parallel

In order to increase the speed of decoding MPEG video data to provide the video data for more applications, one embodiment provides parallel decoding of the video data among multiple processors in a single system, sharing a memory. In particular, in one embodiment, the workload of decoding the video data is distributed among the set of processors at the slice level. In alternative embodiments, the workload of decoding the video data could be distributed among the set of processors at a level other than the slice level, without departing from the present invention.

In particular, as defined by the standard, a slice in MPEG is a series of an arbitrary number of macroblocks within one row of the picture. Figure 3 illustrates a general slice structure. Each slice contains at least one macroblock, and consecutive slices may not overlap. Slices occur in the bitstream in the order in which they are encountered, starting at the upper-left of the picture and proceeding by raster-scan order from left to right and top to bottom. However, slices do not need to maintain the same structure from picture to picture: there may be different numbers of slices and/or different slice sizes.

Figure 4 is a flow diagram describing the steps of decoding the video data among multiple processors in parallel, according to one embodiment. In step 402 a first processor executing a first process, scans/reads a video sequence into memory from a disk or some other source of compressed video.

In step 404, the first processor further reads the video sequence to identify slice startcodes to identify the beginning of slices within the video sequence. In step 406, the first processor further reads the macroblocks within each slice to estimate the workload associated with decoding a respective slice.

In step 408, the first processor assigns one or more slices to be decoded, to each processor within a group of processors included in a

system. In one embodiment, the slices are assigned to the different processors in a manner to spread the workload evenly among the processors. For example, if a first slice includes many macroblocks, it presumably will take longer to decode. Therefore, a second processor would be assigned fewer slices to decode because at least one slice presumably will take longer to decode. Subsequent adjacent slices may include significantly less macroblocks. Therefore, a third processor, may be assigned more slices to decode, with each slice containing less macroblocks. In the end, each of the processors, in one embodiment, is to receive a comparable workload of slices to decode.

In step 410, the first processor writes in a shared memory, the first and last assigned slices as local variables for each of the processors that are provided to decode the slices. For example, if the second processor is to decode slices 1-3, a third processor to decode slices 4-8, and a fourth processor decode slices 9-12, the slice numbers are written in memory as local variables for each of the respective processors. One benefit to assigning the slices by identifying the slices as local variables for the respective processors, as opposed to providing the slices in a jointly accessible task/slice queue, is the avoidance of conflicts between processors in accessing the queue to identify slices to be decoded.

For example, in the case of using a slice queue, once a processor is done decoding a slice it would return to the queue to determine the next

slice to be decoded. In addition, the processor would also increment a pointer identifying the next slice to be decoded so that the next time a processor accesses the queue it will receive the subsequent slice to be decoded. Moreover, the queue would be accessed fairly frequent. As a result, conflicts between the processors accessing the queue would also be frequent. However, by assigning the slices to be decoded as local variables for each of the respective processors, conflicts between the processors in accessing the memory is significantly decreased.

In step 412, the respective processors read their respective local variables to determine which slices are to be decoded, and thereafter read the slices from memory and decode the slices in accordance with the decoding procedures discussed above. In one embodiment, the processor that assigns the slices to be decoded also assigns to it's self, one or more slices to be decoded, which the processor thereafter proceeds to decode along with the other processors. Moreover, in one embodiment, the respective processors perform the steps of decoding the slices by executing software routines stored in memory, provided for performing the decoding steps as discussed above (e.g., Huffman decoding, Run length decoding, etc.).

Thereafter, the first processor continues to scan/read in the video data and assign contiguous slices to the processors for decoding, for the desired quantity of video that is to be decoded. Furthermore, the method

of decoding the video data by distributing the workload among multiple processors, as described above, can be performed in real-time.

Figure 5 illustrates a system that is capable of decoding multiple slices in parallel with multiple processors, according to one embodiment. As illustrated, the system includes multiple processors sharing a memory (e.g., Symmetric Multiple Processor architecture). In an alternative embodiment, the multiple processors could access separate memories, rather than sharing the same memory, without departing from the present invention.

Moreover, as shown in the memory of the system in Figure 5, the unit of logic to perform the method of decoding the video data through the use of multiple processors in parallel, as described above, could be provided a set of computer instructions to be executed by one or more of the processors. In addition, the logic to perform the steps of decoding the video data could also be provided/stored in memory as a set of computer instructions (e.g. MPEG decoder). The instructions to perform the methods as described above could alternatively be stored on other forms of computer/machine readable medium, including magnetic and optical disks. For example, method of the present invention can be stored on computer/machine readable mediums, such as magnetic disks or optical

disks, that are accessible via a disk drive (or computer-readable medium drive), such as the disk drive shown in Figure 5.

Alternatively, the logic to perform the methods as discussed above, including the method of decoding video data via multiple processors in parallel, could be implemented in additional computer and/or machine readable mediums, such as discrete hardware components such as large-scale integrated circuits (LSI's), application-specific integrated circuits (ASIC's), firmware such as electrically erasable programmable read-only memory (EEPROM's); and, electrical, optical, acoustical or other forms of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.).

CLAIMS

What is claimed is:

1. A method for decoding compressed video comprising:

reading a stream of compressed video into a memory, said video having multiple pictures, each picture having one or more independent elements;

assigning, via a first processor of a group of processors sharing said memory, at least one independent element per processor to be decoded by the processors in parallel; and

decoding the independent elements of the video in parallel.

2. The method of claim 1, wherein the independent elements include slices.

3. The method of claim 2, wherein assigning the independent elements includes assigning a varying number of slices to individual processors.

4. The method of claim 3, wherein assigning the independent elements includes assigning a comparable work load to the processors.

5. The method of claim 4, wherein assigning the independent elements includes placing in memory as a local variable, for each processor, the slices to be decoded by a respective processor.

6. The method of claim 5, wherein each slice includes at least one macroblock.

7. The method of claim 6, wherein said video is encoded in MPEG.

8. The method of claim 7, wherein the method of decoding is performed in real-time.

9. A computer-readable medium having stored thereon a set of instructions, said set of instruction for decoding compressed video, which when executed by a processor, cause said processor to perform a method comprising:

reading a stream of compressed video into a memory, said video having multiple pictures, each picture having one or more independent elements;

assigning, via a first processor of a group of processors sharing said memory, at least one independent element per processor to be decoded by the processors in parallel; and

decoding the independent elements of the video in parallel.

10. The computer-readable medium of claim 9, wherein the independent elements include slices.

11. The computer-readable medium of claim 10, wherein assigning the independent elements includes assigning a varying number of slices to individual processors.

12. The computer-readable medium of claim 11, wherein assigning the independent elements includes assigning a comparable work load to the processors.

13. The computer-readable medium of claim 12, wherein assigning the independent elements includes placing in memory as a local variable, for each processor, the slices to be decoded by a respective processor.

14. The computer-readable medium of claim 13, wherein each slice includes at least one macroblock.

15. The computer-readable medium of claim 14, wherein said video is encoded in MPEG standard.

16. The computer-readable medium of claim 15, wherein the method of decoding is performed in real-time.

17. A computer system comprising:

a plurality of processors ;

a memory coupled to said plurality of processors;

a first unit of logic to read a stream of compressed video into said memory, said video having multiple pictures, with each picture having one or more independent elements; and

said first unit of logic further assigns, via a first processor of said group of processors sharing said memory, at least one independent element per processor to be decoded by the processors in parallel.

18. The computer system of claim 17, wherein the independent elements include slices.

19. The computer system of claim 18, wherein said first unit of logic assigns a varying number of slices to individual processors.

20. The computer system of claim 19, wherein said first unit of logic assigns a comparable work load to the processors.

21. The computer system of claim 20, wherein said first unit of logic places in memory as a local variable, for each processor, the slices to be decoded by a respective processor.

22. The computer system of claim 21, wherein each slice includes at least one macroblock.

23. The computer system of claim 22, wherein said video is encoded in MPEG standard.

24. The computer system of claim 23, wherein system computer system decodes said video in real-time.

ABSTRACT OF THE DISCLOSURE

A method and apparatus for decoding compressed video. The method includes reading a stream of compressed video into a memory. The video includes multiple pictures, with each picture having one or more independent elements. Thereafter, assigning, via a first processor of a group of processors sharing the memory, at least one independent element per processor to be decoded by the processors in parallel; and decoding the independent elements of the video stream in parallel.

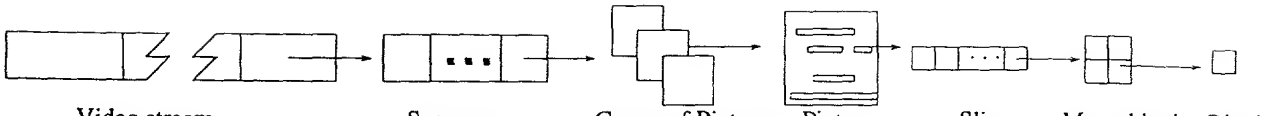
Video stream
Sequence
Group of Pictures
Picture
Slice
Macroblock
Block

Fig 1

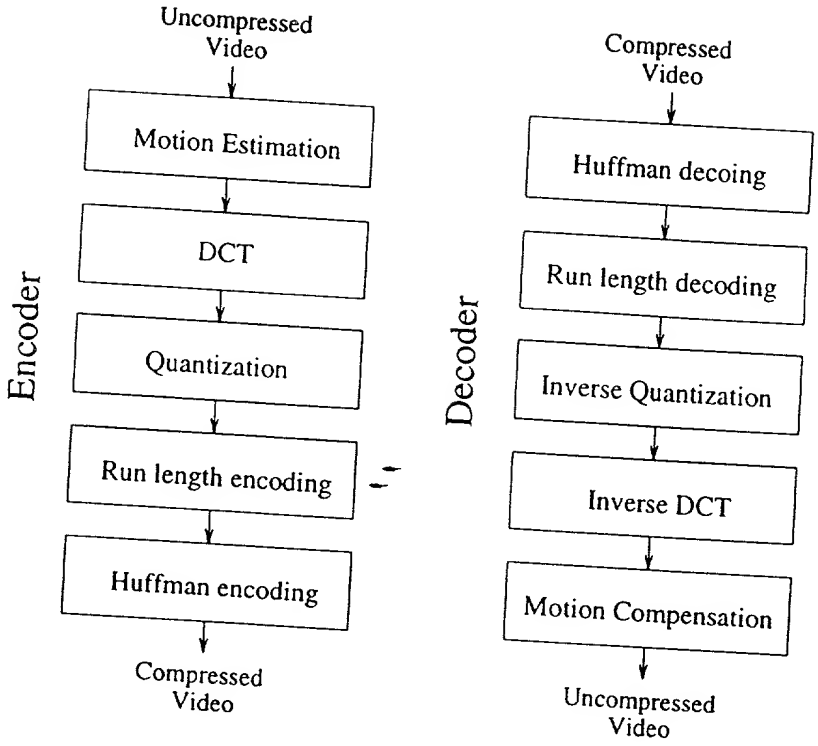
Encoder
Uncompressed Video
Motion Estimation
DCT
Quantization
Run length encoding
Huffman encoding
Compressed Video
Decoder
Compressed Video
Huffman decoing
Run length decoding
Inverse Quantization
Inverse DCT
Motion Compensation
Uncompressed Video

FIG. 2

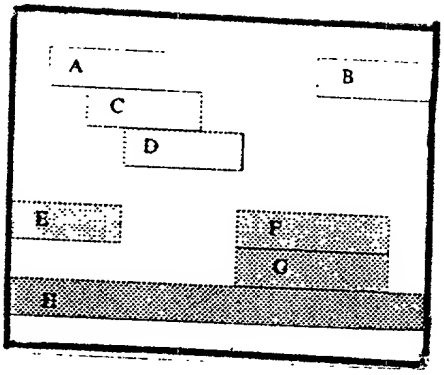

Fig. 3

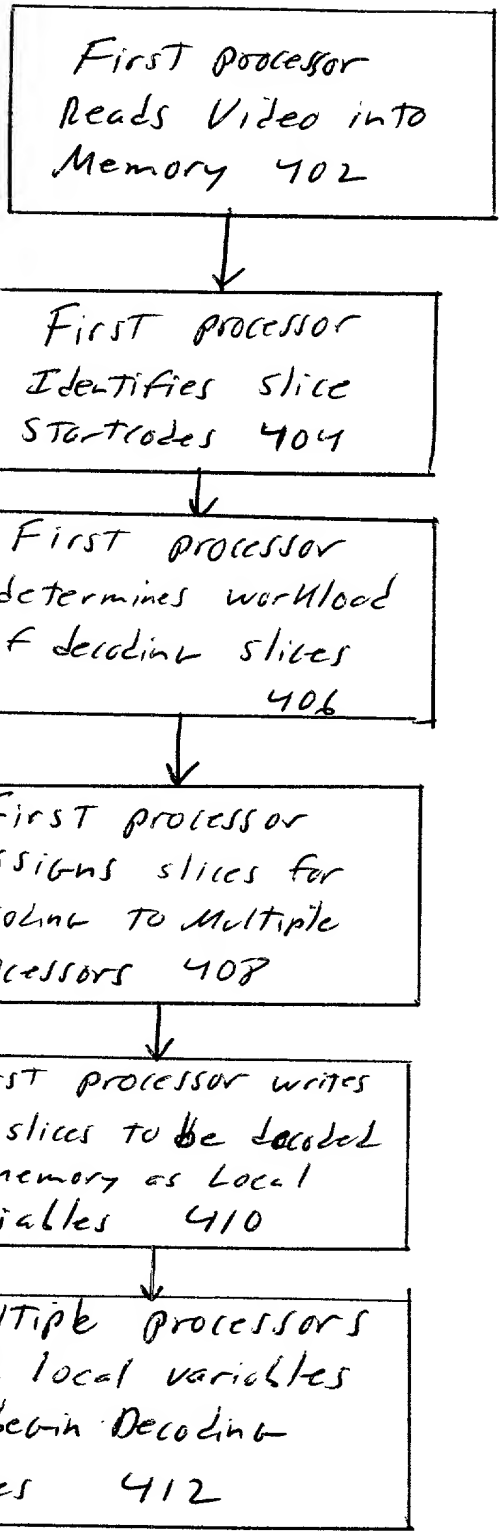
First processor Reads Video into Memory 402
First processor Identifies slice STartcodes 404
First processor determines workload of decoding slices 406
First processor assigns slices for decoding to Multiple Processors 408
First processor writes the slices to be decoded in memory as Local variables 410
Multiple processors read local variables to begin Decoding Slices 412

FIG. 4

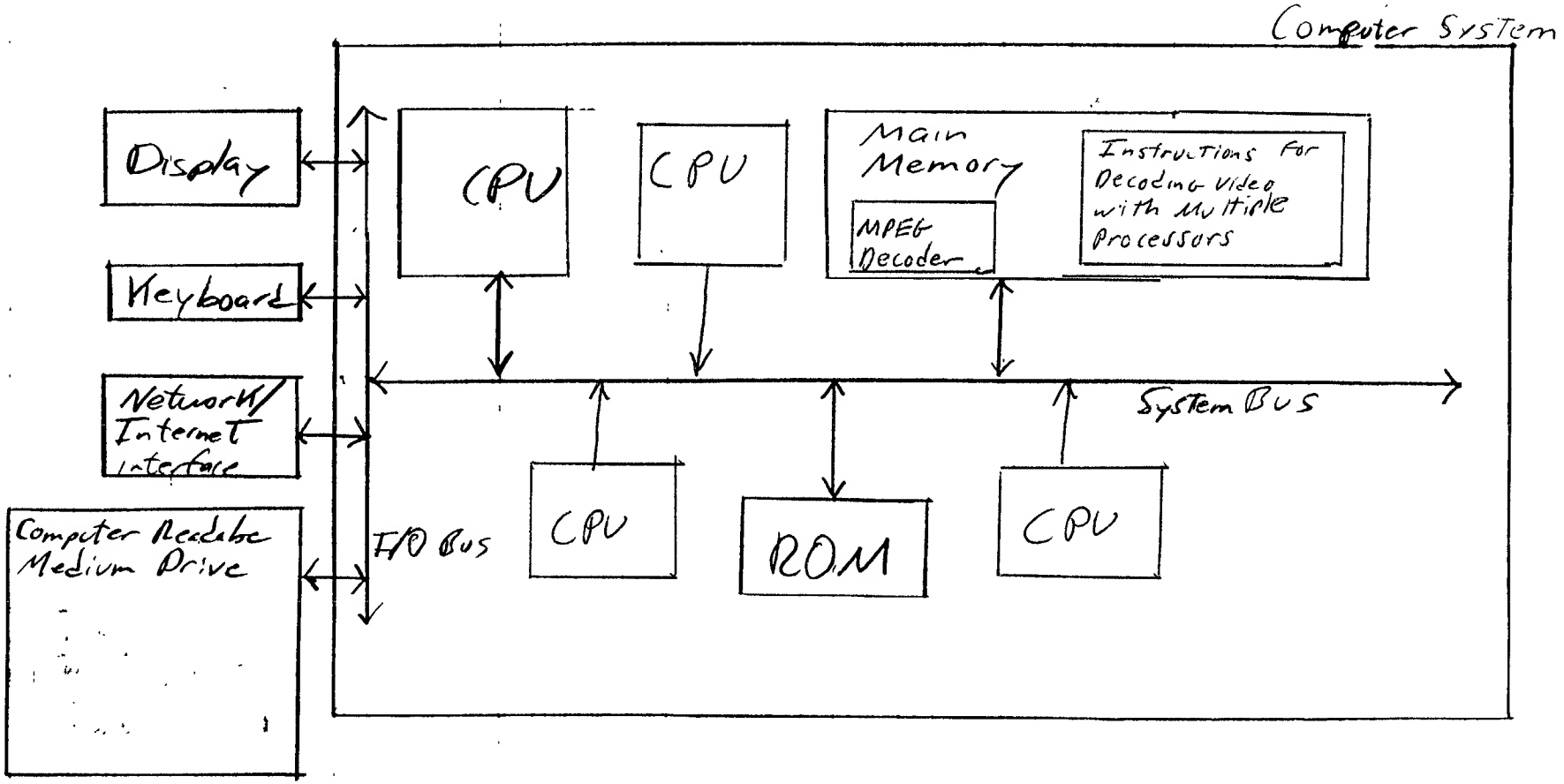
Computer System
Display
Keyboard
Network/ Internet Interface
Computer Readable Medium Drive
CPU
CPU
Main Memory
MPEG Decoder
Instructions for Decoding Video with Multiple Processors
System Bus
I/O Bus
CPU
ROM
CPU

FIG. 5

Attorney's Docket No.: 042390.P7940 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND APPARATUS FOR VIDEO DECODING ON A MULTIPROCESSOR SYSTEM

the specification of which

_X_ is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to John P. Ward **(Name of Attorney or Agent)**, **BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to** John P. Ward **(Name of Attorney or Agent)**, **(408) 720-8598.**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature _____ Date _____

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Inventor's Signature [signature] Date Dec 22 1999

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APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.